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MULTIPLE TRANSMIT DATA RATES IN PROGRAMMABLE LOGIC DEVICE SERIAL INTERFACE

Background of the Invention

[0001] This invention relates to a multiple channel high-speed serial interface, especially in a programmable logic device, in which different channels may have different transmit data rates.

[0002] Recently, PLDs have begun to incorporate high-speed serial interfaces to accommodate high-speed (i.e., greater than 1 Gbps) serial I/O standards -- e.g., the XAUI (10 Gbps Extended Attachment Unit Interface) standard. In accordance with the XAUI standard, a high-speed serial interface includes transceiver groups known as "quads," each of which includes four transceivers and some central logic. Within each transceiver, the receiver portion typically includes a phase-locked loop ("PLL"), primarily for the purpose of enabling clock data recovery from a received high-speed serial signal. In addition, the central logic typically includes a PLL, primarily for the purpose of generating a transmit clock to be used by the transmitter portion of each of the four transceivers, and in some cases for generating a reference clock for the receiver PLLs.

[0003] In many cases, the individual receivers or transmitters in a quad are intended to be used together, for multi-channel reception or transmission of related signals. In such applications, there is no disadvantage

in having a common transmit clock generated in the central logic. However, particularly in programmable logic where the use to which a user puts portions of the device may be unexpected, in some applications the individual channels may be used separately, and it may be desirable to be able to use different transmit clocks in the different channels of the quad.

Summary of the Invention

[0004] The present invention provides high-speed serial interface circuitry on a programmable logic device with the ability for different channels to use different transmit clocks based on a common clock source. This is achieved by providing in each channel one or more dividers that can divide the common clock by one or more integer values, providing one or more clocks that are "integer fractions" of the common clock -- i.e., one or more clocks of which the common clock is an integer multiple.

[0005] In one preferred embodiment, the central logic of each quad of the serial interface has a single PLL or other clock source to provide a transmit clock, and each channel in that quad has one divider for optionally providing, under control of the user, or under control of logic in the programmable logic core of the PLD, a clock that is an integer fraction of the common clock.

[0006] The number of variations on that preferred embodiment are limited only by the device area which one is prepared to devote to the serial interface. Thus, in another preferred embodiment, the divider in each channel may provide a programmable selection of two or more integers by which to divide the common clock, although such a divider would consume more device area than a divider capable of division by only one integer. In a further embodiment, one or more channels may have more than one such divider. In one variant of that further embodiment, all dividers in a channel with more than one divider may provide the same selection of integers by

which to divide the common clock. In another variant of that further embodiment, each divider in a channel with more than one divider may provide a different selection of integers by which to divide the clock. In any of these embodiments and variants, all channels can be equipped with the a divider or set of dividers providing the same integer or set of integers by which the common clock may be divided, or different channels can be equipped with different dividers or sets of dividers providing different integers or sets of integers by which the common clock may be divided.

[0007] In the embodiments and variants thus far described, each quad has a single common clock. However, and again depending on the available device area, it may be possible in another embodiment to provide a second common clock source (or even further additional common clock sources). In such a case, the divider or dividers in each channel could be replicated for each common clock source, or a selection device, such as a multiplexer, could be provided allowing selection of a particular common clock source for input into a particular divider. Thus, in one preferred embodiment, there may be two common clock sources in a single central control circuitry. If the number of clock rates needed exceeds those that can be provided using integer fractions of the clock or clocks provided in the central control circuitry, additional clocks may be provided in the central control circuitry of another quad, if present.

[0008] Regardless of the number of common clock sources, where there is more than one divider provided, a selection device, such as a multiplexer, could be provided in each channel allowing selection of the output of a particular divider as the transmit clock for that channel. Even if a channel has only a single divider, a multiplexer may be provided to allow selection between the divider output and the undivided common clock (although this would not be necessary where the divider is one, as is described

above, that allows a choice among multiple integers and one of those integers is 1).

[0009] High-speed serial interfaces of the type being discussed commonly are used to convert high-speed serial data to parallel data for use in a device, such as a programmable logic device, that operates in parallel mode. Therefore, it is common for such a high-speed serial interface to include a divider in the central control circuitry for providing a parallel clock which is an integer fraction of the common clock, which itself is provided as a serial clock. The integer fraction generally reflects the number of bits per byte. In such an interface, the common clock provided by the central control circuitry to the individual channels is actually two common clocks --one serial and one parallel. By extension, every divider provided in one of the channels as discussed above, for converting the common clock to a channel clock, may actually be two clocks -- one for converting the serial clock from the common serial clock rate to the channel serial clock rate, and one for converting the parallel clock from the common parallel clock rate to the channel parallel clock rate. Alternatively, the local parallel clock may be derived from the locally divided serial clock by a further local divider.

[0010] Thus, in accordance with the present invention, there is provided a serial interface for use in a programmable logic device. The serial interface includes a plurality of channels, each of the channels including at least transmit circuitry. The interface also includes central control circuitry including at least one clock source for generating at least one transmit clock for use by the transmit circuitry in each of the channels. Each such transmit clock has a respective first clock rate. Clock division circuitry in at least one of the channels provides from each such transmit clock a channel-derived clock having a second clock rate at most equal to the

first clock rate. A programmable logic device incorporating such an interface is also provided.

Brief Description of the Drawings

[0011] The above and other advantages of the invention will be apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout, and in which:

[0012] FIG. 1 is a block diagram of a preferred embodiment of a programmable logic device incorporating the present invention;

[0013] FIG. 2 is a schematic diagram of a serial interface incorporating the present invention;

[0014] FIG. 3 is a schematic diagram showing detail of the central control circuitry and two transceivers of one quad of a first preferred embodiment of the interface of FIG. 2;

[0015] FIG. 4 is a schematic diagram showing detail of the central control circuitry and one transceiver of one quad of a second preferred embodiment of the interface of FIG. 2; and

[0016] FIG. 5 is a simplified block diagram of an illustrative system employing a programmable logic device incorporating a serial interface in accordance with the present invention.

Detailed Description of the Invention

[0017] As described above, the present invention provides multiple transmit clocks for each individual channel of a high-speed serial interface from a smaller number of transmit clocks generated centrally in each quad of the interface. The multiple clocks are provided by dividing a centrally generated clock in a given quad. Preferably, each channel includes its own divider or dividers for generating whatever channel clocks it may need.

[0018] The use of dividers to generate the channel clocks limits the channel clocks to integer fractions (as defined above) of the centrally generated clock. Where other clocks may be needed that are not integer fractions of a single central clock, a second central clock may be provided that also can be divided to provide additional channel clocks. If device area is not a concern, still more central clocks can be provided. However, in a preferred embodiment, at most two central clocks are provided, and if any clock is needed that cannot be derived by division of those two clocks, then that clock can be provided in a separate quad, if present.

[0019] The invention will now be described with reference to FIGS. 1-4.

[0020] PLD 10, shown schematically in FIG. 1, is one example of a device incorporating a serial interface 20 according to the invention. PLD 10 has a programmable logic core including programmable logic regions 11 accessible to programmable interconnect structure 12. The layout of regions 11 and interconnect structure 12 as shown in FIG. 1 is intended to be schematic only, as many actual arrangements are known to, or may be created by, those of ordinary skill in the art.

[0021] PLD 10 also includes a plurality of other input/output ("I/O") regions 13. I/O regions 13 preferably are programmable, allowing the selection of one of a number of possible I/O signaling schemes, which may include differential and/or non-differential signaling schemes. Alternatively, I/O regions 13 may be fixed, each allowing only a particular signaling scheme. In some embodiments, a number of different types of fixed I/O regions 13 may be provided, so that while an individual region 13 does not allow a selection of signaling schemes, nevertheless PLD 10 as a whole does allow such a selection.

[0022] For example, each I/O region 20 preferably is a high-speed serial interface as described above, similar to an interface capable of implementing the XAUI standard. Thus, as shown in FIG. 2, each interface 20 preferably

includes one or more groupings 200, 201 having four channels 21-24, each including a transmitter 25 and a receiver 26, as well as central logic 27. As discussed above, because each such grouping includes four channels, it may be referred to as a "quad." However, it should be understood that in accordance with the present invention, which is not linked to any particular high-speed serial standard, each grouping 200, 201 can include any number of channels. Similarly, while each region 20 is shown to contain two groupings 200, 201, each region 20 may contain any number of groupings 200, 201.

[0023] As shown in FIG. 1, PLD 10 includes five interfaces 20. However, PLD 10 may include any desired number of interfaces 20, with a corresponding number of channels.

[0024] Within each interface 20, all transmitters 25 preferably are substantially identical, and all receivers 26 preferably are substantially identical, and preferably are substantially similar to known high-speed serial interface transmitters and receivers such as those used with the XAUI standard. Preferably the only differences among transmitters 25 are that each may have a different number or type of clock divider in accordance with the present invention, as discussed above and with reference to the drawings below. It further should be noted that any differences between transmitter 25 or receiver 26 and known high-speed serial transmitters and receivers preferably maintain compatibility with existing standards such as the XAUI standard, while adding capabilities as described herein.

[0025] FIG. 3 shows schematically central logic 27, as well as channels 23, 24, of quad 200. With respect to channels 23, 24, FIG. 3 particularly shows a portion of each transmitter 25. As seen in FIG. 3, central logic 27 includes PLL 30 for generating a central serial transmit clock (SCLK) 31, and a divider 32 for dividing down central serial transmit clock 31 to provide central parallel transmit clock (PCLK) 33. For example,

divider 32 typically will divide central serial clock 31 by 8 or 10 to reflect the number of bits in a byte, providing a central parallel clock 33 having a rate one-eighth or one-tenth that of central serial clock 31. However, other divisors can be used as required by the particular application.

[0026] As depicted in FIG. 3, in transmitter 25 of each channel 23, 24, both serial clock 31 and parallel clock 33 are input to respective dividers 34, 35, 36, 37. As shown in FIG. 3, all four dividers 34-37 are capable of dividing their respective input clocks by factors of 1, 2 or 4. Which factor is used may be programmed by the user when programming the rest of PLD 10, or user logic in the PLD core (see FIG. 2) could control any or all of dividers 34-37 via leads 38. Normally one would expect two dividers in the same transmitter 25 (e.g., dividers 34, 35 in channel 23 that derive SCLK' and PCLK', and dividers 36, 37 in channel 24 that derive SCLK" and PCLK") to be set to the same divisor, to maintain the same serial/parallel relationship as clocks 31, 33, although there may be applications where that is not the case. On the other hand, however, one would not be surprised to have the dividers in different channels -- even where, as in FIG. 3, the choices of divisors is the same -- set to different divisors, although there may be applications where all channels are similarly set. Moreover, there may be embodiments where the choices of divisors are not the same in each channel 23, 24, or even within a single channel, where flexibility to use different clock rates is necessary or desirable. In addition, if device area is not a concern, additional dividers with other choices of divisors, or bigger dividers with more choices of divisors, can also be provided (not shown) in one or more channels.

[0027] FIG. 4 shows an arrangement affording even greater flexibility in providing different clock rates. FIG. 4 shows an alternative embodiment 40 of a portion of central logic 27, as well as an alternative embodiment 41

of a portion of transmitter 25 of channel 22. Central logic 40 has two clock sources (e.g., PLLs) 42, 43 providing respective high-speed serial clocks (SCLK0, SCLK1) 420, 430. Dividers 44, 45 derive respective parallel clocks (PCLK0, PCLK1) 421, 431 from serial clocks 420, 430. All of clocks 420, 421, 430, 431 are made available to the various channels. It should be noted that while FIG. 4 shows two central clock sources, any number of central clock sources may be provided within the area constraints of PLD 10, depending on how much of PLD 10 one is willing to devote to additional clock sources. If any application requires more clock choices than are provided in a single quad 200, additional clocks may be provided in a second quad 201, if present.

[0028] As seen, physical medium attachment ("PMA") portion 410 of transmitter 41 has two dividers 411, 412, which are used to divide serial clocks 420, 430, respectively. Again, as in FIG. 3, both dividers 411, 412 provide the same choice of divisors (1, 2, 4), although the choices provided by the two different dividers could be different, and more dividers or bigger dividers with additional divisors can be provided. And as again also seen in FIG. 3, the selection of which divisor is used by each divider 411, 412 may be made by user programming of PLD 10 or by user logic in the PLD core via lead 38. The choice of whether the output of divider 411 (divided clock 420) or divider 412 (divided clock 430) is used in PMA 410 is made by multiplexer 413, based on user programming or core logic control (via lead 48). The serial clock selected by multiplexer 413 is provided to serializer 400 on lead 401.

[0029] The serial clock selected by multiplexer 413 also is provided to divider 414 to generate a corresponding parallel clock, although the parallel clock also could be generated, as in FIG. 3, by providing additional dividers (not shown), corresponding to dividers 411, 412, respectively, on centrally generated parallel clocks 421, 431. Similarly, in the embodiment of

FIG. 3, the parallel clock in each channel could be derived, as here in FIG. 4, by first deriving the local serial clock using divider 34 or 36, and then dividing that local serial clock using a divider (not shown) to derive a local parallel clock.

[0030] The parallel clock 415 generated by divider 414 preferably is selected by multiplexer 416 and provided to serializer 400 on lead 402. Clock 415 preferably also is fed back to physical coding sublayer ("PCS") portion 440 of transmitter 41 which uses clock 415 to provide to serializer 400 the data to be serialized.

[0031] It should be noted that interface 20 also could be operated in a mode (e.g., when using the XAUI standard) in which all channels operate synchronously. In such a case, one of clocks 420, 430 will be used as the serial clock and the corresponding parallel clock 421 or 431 will be used. In such a case, divider 411 or 412 will be set to divide by 1 to provide the serial clock, and to enhance synchronization, centrally provided parallel clock 421 or 431 will be selected by multiplexer 416 and provided to serializer 400, rather than using divider 414 to provide the parallel clock. In this case, multiplexer 441 of PCS 440 will select the centrally generated parallel clock provided to all channels by multiplexer 46, and will ignore the parallel clock selected by multiplexer 416. Even though multiplexer 416 in this case is selecting the same centrally generated clock, there is less skew if PCS 440 of each channel receives the parallel clock directly, without the clock having to pass through respective PMA 410.

[0032] A PLD 10 incorporating interfaces 20 according to the present invention may be used in many kinds of electronic devices. One possible use is in a data processing system 120 shown in FIG. 5. Data processing system 120 may include one or more of the following components: a processor 121; memory 122; I/O circuitry 123; and peripheral devices 1244. These components are coupled together by a system bus 125 and

are populated on a circuit board 126 which is contained in an end-user system 127.

[0033] System 120 can be used in a wide variety of applications, such as computer networking, data networking, instrumentation, video processing, digital signal processing, or any other application where the advantage of using programmable or reprogrammable logic is desirable. PLD 10 can be used to perform a variety of different logic functions. For example, PLD 10 can be configured as a processor or controller that works in cooperation with processor 121. PLD 10 may also be used as an arbiter for arbitrating access to a shared resources in system 120. In yet another example, PLD 10 can be configured as an interface between processor 121 and one of the other components in system 120. It should be noted that system 120 is only exemplary, and that the true scope and spirit of the invention should be indicated by the following claims.

[0034] Various technologies can be used to implement PLDs 10 as described above and incorporating this invention.

[0035] It will be understood that the foregoing is only illustrative of the principles of the invention, and that various modifications can be made by those skilled in the art without departing from the scope and spirit of the invention, and the present invention is limited only by the claims that follow.